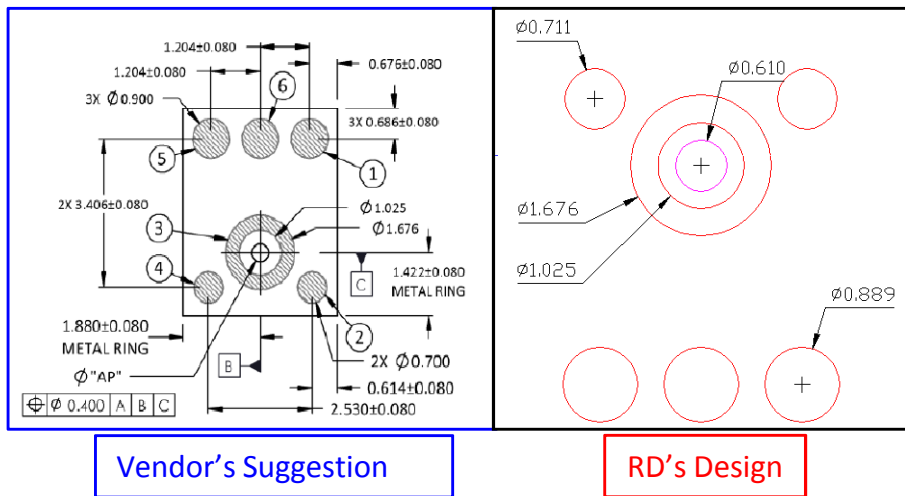
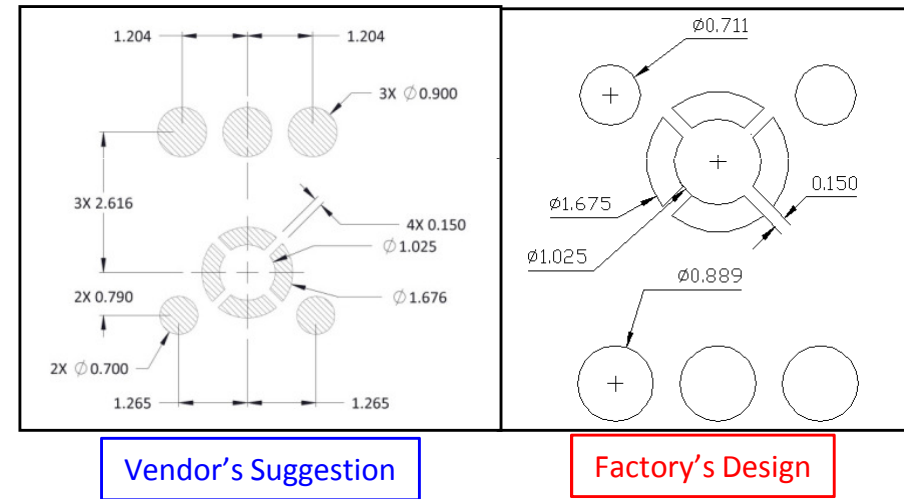


1. PCB LAND PATTERN & SOLDER STENCIL PATTERN:

PCB LAND PATTERN:



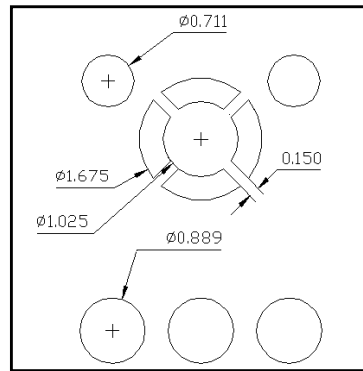
SOLDER STENCIL PATTERN:



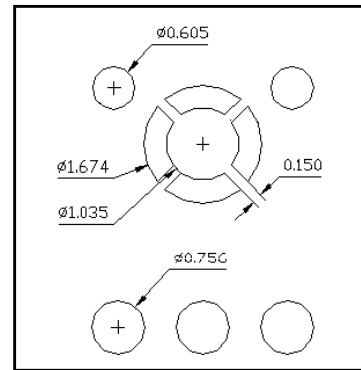
Summary:

- Pad on PCB is similar with Vendor's suggestion
- Aperture stencil was designed base on PCB and Vendor's suggestion

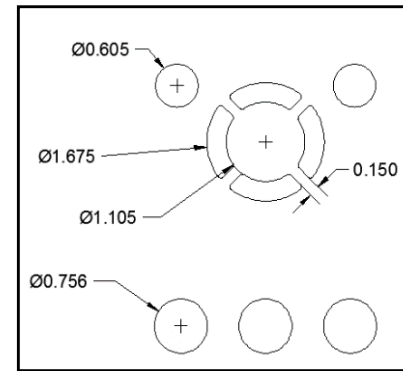
2. STENCIL VERSION HISTORY & ISSUES:



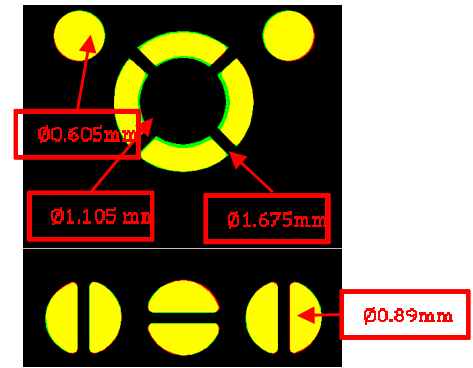
V1: T=0.1mm
Void & solder ball



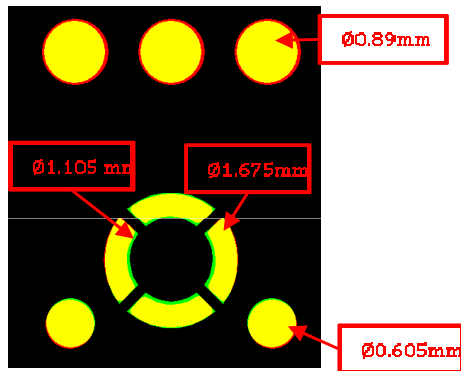
V2: T=0.1mm
Void solder



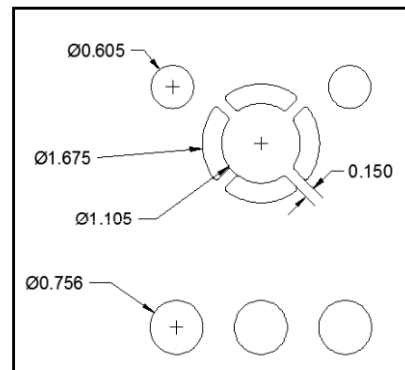
V3-1-1: T=0.08mm
Void & O-ring not seal



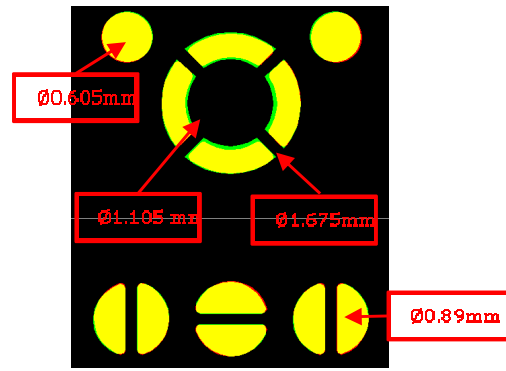
V3-1-2: T=0.08mm
Void & O-ring not seal



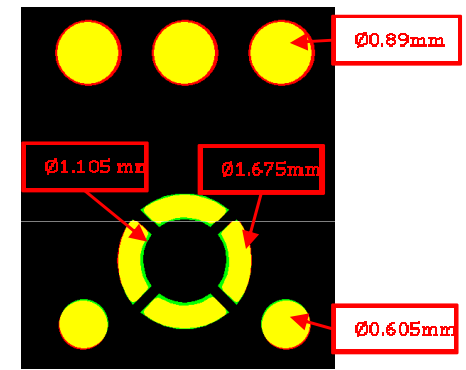
V3-1-3: T=0.08mm
Void & O-ring not seal



V3-2-1: T=0.12mm
Void solder



V3-2-2: T=0.12mm
Void solder



V3-2-3: T=0.12mm
Void solder

V1: DVT1

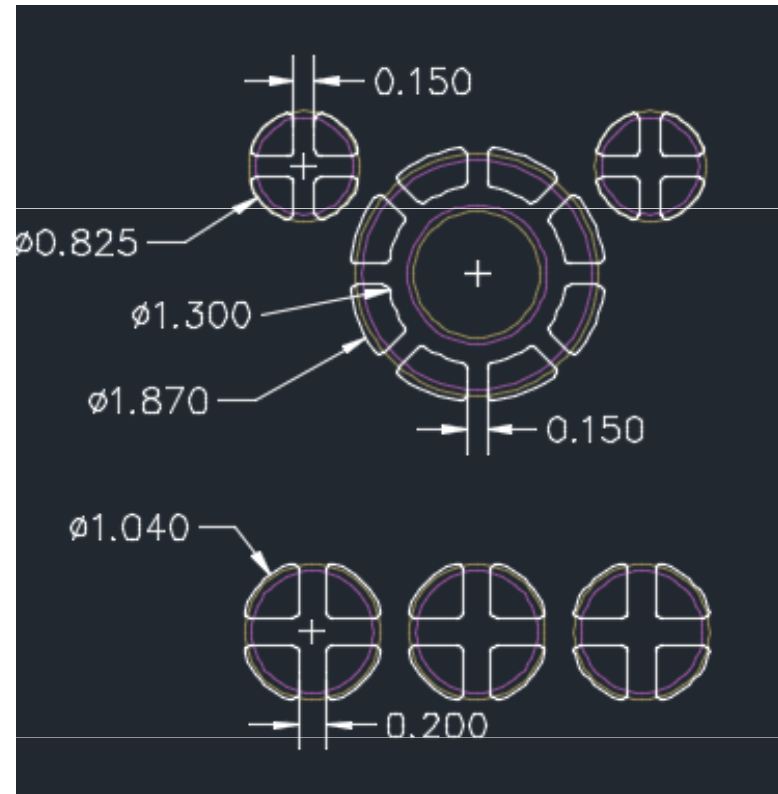
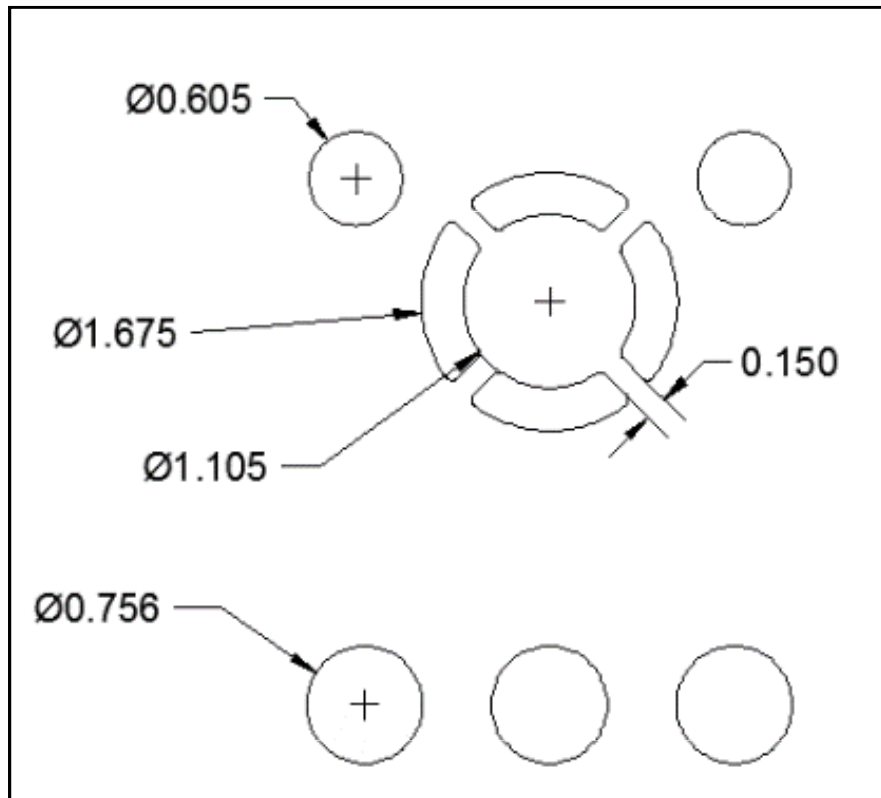
V2: DVT2

V3: DVT3 (factory made 3 kind of stencil with 2 different thickness of solder paste)

Summary:

- After many times to improve stencil: Solder ball/ O-ring seal can be improved but Void solder is still not improved

3. Factory keep to modify aperture stencil to improve void issues in DVT4 build and keep monitor result



- The void soldering specification recommended by the factory:
 - As IPC –A-610 specifications, The void solder is only defined for BGA, without flat pad.
 - Factory suggest to apply specifications as normal components (such as Bottom termination components) for MIC parts: The minimum solder coverage is bigger than 50%

8.3.13 Bottom Termination Components (BTC)

Some other names for these devices are Land Grid Array (LGA), Quad Flat No-Lead (QFN), Plastic Quad Flat No-Lead (PQFN), Microlead Frame Packages (MLF), Leadless Plastic Chip Carriers (LPCC), and Quad Flat No-Lead Exposed Pad (QFN-EP). Connections formed to bottom termination components (BTC) **shall** meet dimensional and solder fillet requirements in Table 8-16, see Figures 8-174 and 175.

Bottom Termination Component (BTC) process guidance is provided in IPC-7093, which contains recommendations developed from extensive discussion of BTC process development issues.

Process development and control is essential for continued success of assembly methods and implementation of materials. Process validation and control can be used in lieu of X-ray/visual inspection provided objective evidence of compliance is available.

Thermal plane void criteria **shall** be established between the Manufacturer and User.

Table 8-16 Dimensional Criteria – BTC

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	A	50% (W), Note 1	25% (W), Note 1	
Toe Overhang (outside edge of component termination)	B	Not permitted		
Minimum End Joint Width	C	50% (W)	75% (W)	
Minimum Side Joint Length	D	Note 4		
Solder Fillet Thickness	G	Note 3		
Minimum Toe (End) Fillet Height	F	Notes 2, 5		
Termination Height	H	Note 5		
Land Width	P	Note 2		
Termination Width	W	Note 2		

Note 1. Does not violate minimum electrical clearance.

Note 2. Unspecified parameter or variable in size as determined by design.

Note 3. Wetting is evident.

Note 4. Not a visually inspectable attribute.

Note 5. (H) = height of solderable surface of lead, if present. Some package configurations do not have a continuous solderable surface on the sides and do not require a toe (end) fillet.

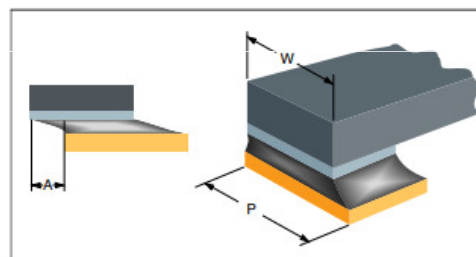


Figure 8-8

Target – Class 1,2,3

- No side overhang.

Acceptable – Class 1,2

- Side overhang (A) is less than or equal to 50% width of component termination area (W) or 50% width of land (P), whichever is less.

Acceptable – Class 3

- Side overhang (A) is less than or equal to 25% width of component termination area (W) or 25% width of land (P), whichever is less.

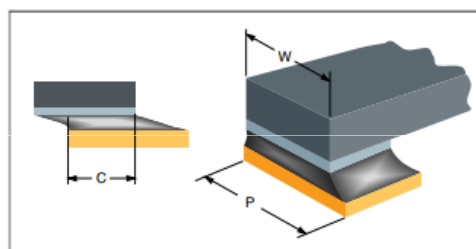


Figure 8-10

Target – Class 1,2,3

- End joint width (C) is equal to the width of the component termination (W) or width of land (P), whichever is less.

Acceptable – Class 1,2

- Minimum end joint width (C) is 50% width of component termination (W) or 50% width of land (P), whichever is less.

Acceptable – Class 3

- Minimum end joint width (C) is 75% width of component termination (W) or 75% width of land (P), whichever is less.

Does not violate minimum electrical clearance